

## Socionext to Showcase Leading-Edge SoC Design Solutions at DesignCon 2020

*Featuring Data Center High-Performance ASIC, Advanced Packaging Technology, ADC for 5G Wireless, and Computer Vision AI*

**Langen/Germany, 23. January, 2020** --- Socionext Inc., a world leading silicon supplier, will feature its advanced SoC designs including 112G SerDes, 120+ GS/s ADC/DAC, PCIe Gen5, high-performance memory, multi-die package design solutions, and AI technology at the annual DesignCon conference, Jan. 28 – 30, at the Santa Clara Convention Center, Booth 1234.

AI applications running on the cloud data center demand greater interconnect bandwidth, larger on-chip memory, and ultra-low latency. Socionext provides extended 2.5/3D HBM+, multi-die packaging, and advanced process node solutions for meeting and exceeding these emerging requirements.

At this year's DesignCon, Daniel Lambalot, Director of Engineering at Socionext, along with experts from Micron and Cadence Design Systems, will be addressing such design complexity by delivering a presentation on "Designing Next Generation Memory Interfaces: Modeling, Analysis, and Tips" on Wednesday, Jan 29, 2020 from 2:00-2:45 PM at Ballroom A.

See <https://schedule.designcon.com/session/designing-next-generation-memory-interfaces-modeling-analysis-tips/868327> for more information.

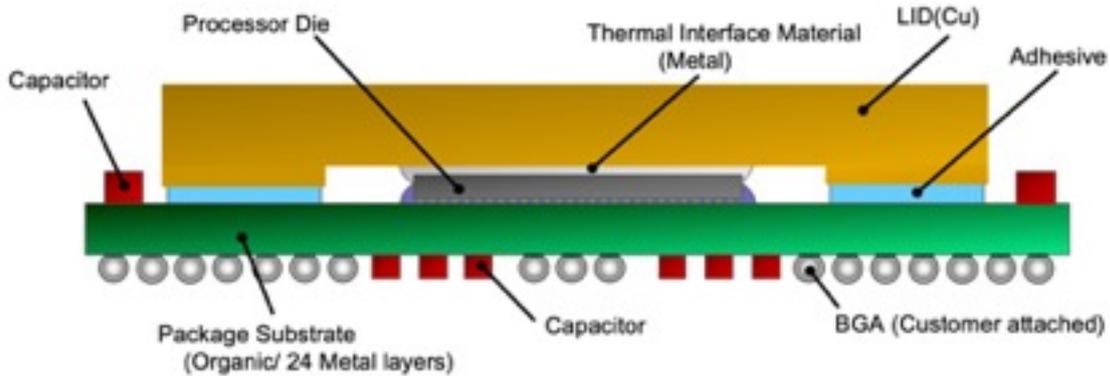
Additionally, two members from Socionext will be presenting at the Ansys booth 745 (<https://www.ansys.com/other/designcon>). On Thursday, Jan 30 at 3:00 PM, Daniel Lambalot will explain challenges of designing 112Gbps channels via a presentation titled "Modelling and measurement correlation for a 112Gbps package + PCB using HFSS and SIWave with HFSS regions". On the same day at 4:30 PM, Takafumi Shimada, Electromagnetic Analysis Specialist at Socionext, will present "Automating the Multi-Physics Simulation Process for LSI-Package-Board" and introduce Socionext's latest simulation automation and parametrics verification process of pre-design interconnects.

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### Sample of an FC-PBGA CPU Design for High-end Server

[\(view larger image\)](#)

Socionext will showcase superior-quality, high-performance, multi-die package methodology and designs. Offerings include FanOut Wafer Level Packaging (FOWLP), RF/mmWave solutions, and multi-die chiplets supporting a wide range of process nodes, interconnect and die-to-die (D2D) interface. Furthermore, Socionext offers Antenna-in-Package (AiP) which addresses the needs of the IoT and 5G telecom markets requiring miniaturization and antenna integration to the same package over the silicon. Socionext's advanced packaging capabilities help companies quickly and cost-effectively fulfill their complex packaging requirements.

Socionext offers a high-performance SerDes macro with up to 112Gbps per channel for up to 400G networks. These capabilities are further extended by utilizing the company's ultra-high-speed ADC & DAC technologies, a key component in coherent and direct detect optical networking SoCs enabling Terabit (Tbps) datacenter interconnect (DCI) solutions for hyperscale cloud operators.

Network providers need to quickly stay ahead of the growing, on-demand, content driven environment with the emergence of 5G. With the need for super-fast AI computational speed and performance, 400G adoption will drive the need for increased PCIe Express bandwidth replacing 100G/200G based network infrastructure. Socionext offers PCIe Gen5 technology for bridging the IO gap between Server CPUs and the host bus adapters that create the 400G network.

"With ASIC development on the rise, Hyperscale cloud service providers expect their vendor to provide a complex SoC along with a full complement of drivers and firmware," said Bob Wheeler, Principal Analyst for Networking at The Linley Group. "ASIC vendors, such as Socionext, now must provide SoC blocks including high-speed interfaces, CPU subsystems, and leading memory interfaces all on the leading process node. "

In addition to offering cutting edge IP, Socionext is developing ASICs on the leading 7nm / 6nm / 5nm process technology. In the mean time, the company is engaging with top foundries to develop products on the next generation technology. Socionext continues to be at the technology forefront in order to support its customers who are using leading edge process nodes for applications in high performance data center and low power mobile devices.

The company will also demonstrate a video solution for analyzing live video streaming. The computer vision system is powered by the Socionext SynQuacer SC2A11, a scalable, ARM®-based multi-core processor, designed to support the most demanding edge computing and real-time data processing applications. It enables real-time video input processing, and provides an easy-to-use interface for managing multiple IP video streams.

Socionext will be raffling great prizes at DesignCon, so stop by booth#1234 to learn more!

For the DesignCon website and programs, visit <http://www.designcon.com/>

### **About Socionext**

Socionext is a global, innovative enterprise that designs, develops and delivers System-on-Chip solutions to customers worldwide. The company is focused on technologies that drive today's leading-edge applications in consumer, automotive and industrial markets. Socionext combines world-class expertise, experience, and an extensive IP portfolio to provide exceptional solutions and ensure a better quality of experience for customers. Founded in 2015, Socionext Inc. is headquartered in Yokohama, and has offices in Japan, Asia, United States and Europe to lead its product development and sales activities. For more information, visit [www.socionext.com/](http://www.socionext.com/).

### **About Socionext America Inc.**

Socionext America Inc. (SNA) is the US branch of Socionext Inc. headquartered in Santa Clara, California. The company is one of the world's leading fabless ASIC suppliers, specializing in a wide range of standard and customizable SoC solutions for automotive, consumer, and industrial markets. Socionext provides customers with quality semiconductor products based on extensive and differentiated IPs, proven design methodologies, and state-of-the-art implementation expertise, with full support.

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