Overview

Socionext has over 40 years’ experience and is a leader in state-of-the-art system-on-chip technology and provides high-performance SoC designs, serial transceiver technologies and advanced packaging solutions. Socionext’s proprietary CHAIS® high-speed converter technology, which allows implementation of extremely fast, high-resolution DAC with low power consumption that can be integrated with millions of gates in standard CMOS process, is the latest in a series of IP offerings.

Developed in TSMC 16FF+ process technology, the high-speed DAC has been designed to cover a broad sampling rate range from 70GSa/s to 120GSa/s (DAC H-family). The high-effective resolution and wide-bandwidth characteristics of previous generations of CHAIS are now supported in a smaller process node, enabling lower power SoC solutions for coherent optical transceivers and high-speed test equipment but is also capable of supporting a whole range of other application areas.

1 CHAIS – CHArge-mode Interleaved Sampler technology

DAC IP Macro Basic Features

- Foundry TSMC
- Technology: 16nm FF+
- Sampling rate (Fs): 70-120GSa/s
- Bandwidth (-3dB): 0.31*Fs
- Typical differential analogue output: 800mVPPDIFF
- Fully programmable and high-performance fractional DPLL
- Available in single channel, IQ pair, 2x IQ pair and 4x IQ pair
- Output clock @Fs/128 to digital core per channel
- Fully specified for -5°C to 100°C operation
- APB control interface
- Silicon proven and used in production, immediately available

Deliverables

- Documentation: datasheet, user guides, test report
- Hard macro & integration support
- Abstract LEF and timing LIB files with constraints
- Behavioral verilog model
- Example test bench
- Layout/package guide

Applications

- High-Speed Communication Systems
- Wireline/Optical Networking
- Wireless/Satellite Communication
- Antenna/Phased-Array/MIMO Systems
- Test & Measurement Equipment
- Industrial and Customer Applications
**DAC IP Macro (H-Family) Part Numbers**

- SNEUDAC120H16 - full rate: 70 - 120GSa/s

For more detailed information on the macro family and support, please contact your Socionext representative.

**Support**

- Development Kit and DAC test chip for customer hands-on experience
- Test program development support
- SI/PI design support

**Development Kit**

Part Number: SNEUADCDAC16H-DK

- 2x ES boards allowing for synchronous operation of 2x DAC & 2x ADC, or 4x ADC, or 4x DAC
- High-performance PCB with optimised analogue interfaces
- On-board Raspberry Pi® including easy to use GUI
- Complete stand-alone system

**Test Chip (ES)**

Evaluation of Socionext’s 16nm CHAIS converters can be conducted via a customized hardware & software platform. Test chips for the 70-120GSa/s 8-bit DAC H-family have 2 DAC channels (one IQ pair). Each of these channels has a capture RAM (waveform memory) to store 512k x 8-bit samples. The RAM contents can be accessed directly via the device SPI interface to the USB/FPGA interface on the accompanying evaluation board. Test chips for the 70-120GSa/s 8-bit DAC family have 2 DAC channels (one IQ pair) and each of these channels has 512k x 8-bit waveform memory.

For more detailed information on the macro family and support, please contact your Socionext representative.