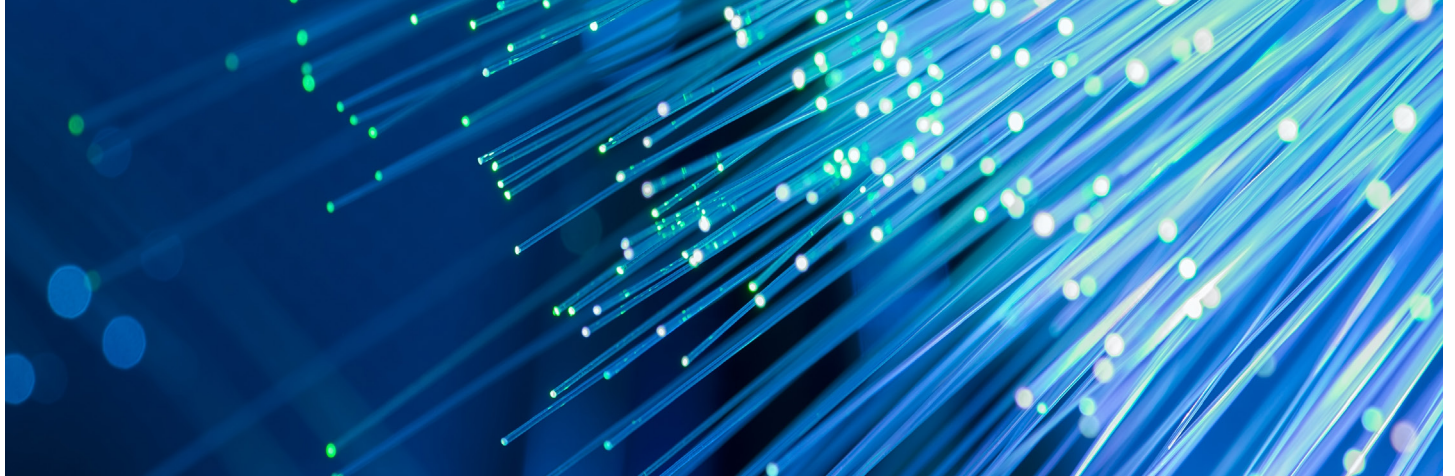


SNEUADCDAC16H Development Kit

15 - 103GSa/s 8-bit ADC H-Family | 70 - 120GSa/s 8-bit DAC H-Family



Overview

Socionext's proprietary CHAIS1 high-speed converter technology is the latest in a series of IP offerings driving advanced systems for fibre optic networks. Developed in TSMC 16FF+ process technology, the high-speed ADC and DAC family has been designed to cover a broad sampling rate range from 15 to 103GSa/s (ADC H-family) and 70 to 120GSa/s (DAC H-family).

The high-effective resolution and wide-bandwidth characteristics of previous generations of CHAIS are supported in a smaller process node, enabling lower power SoC solutions for coherent optical transceivers. The high-effective resolution and wide-bandwidth characteristics of previous generations of CHAIS are now supported in a smaller process node, enabling lower power SoC solutions for coherent optical transceivers and high-speed test equipment but is also capable of supporting a whole range of other application areas.

ADC/DAC Test Chip Features (supported with DKs)

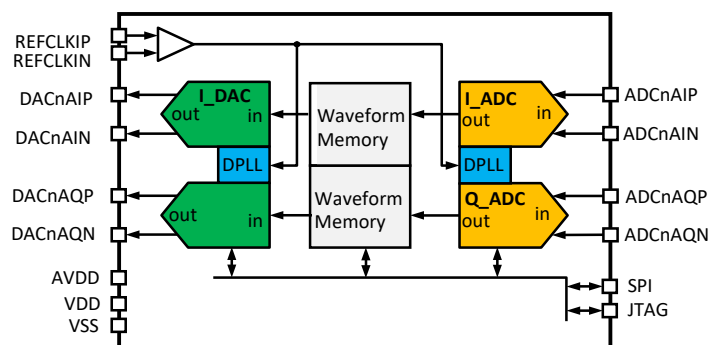
- Technology: 16nm FF+
- Resolution: 8-bit
- Sampling rate (F_s):
 - 70 - 120GSa/s (DAC H-family)
 - 15 - 103GSa/s (ADC H-family)
- Fractional DPLL per IQ pair
- ADC-specific features
 - Programmable analogue input range: 0.5 - 1.7VPPDIFF
- DAC-specific features
 - Typical differential analogue output: 800mVPPDIFF

¹ CHAIS - CHArge-mode Interleaved Sampler technology - which allows implementation of extremely fast, high resolution ADC with low power consumption that can be integrated with millions of gates in standard CMOS process

Test Chip (ES)

Evaluation of Socionext's 16nm CHAIS converters can be conducted via a new customized hardware and software platform. Test chips for the 34 - 120GSa/s 8-bit ADC family have 2 ADC channels (one IQ pair). Each of these channels has a capture RAM to store 512k X 8-bit samples. The RAM contents can be accessed directly via the device SPI interface to the USB/FPGA interface on the accompanying evaluation board. Test chips for the 34 - 120GSa/s 8-bit DAC family have 2 DAC channels (one IQ pair) and each of these channels has 512k x 8-bit waveform memory.

ES Block Diagram



Applications

- High-Speed Communications
- 100G to Terabit Systems
- Test & Measurement Equipment
- Industrial and Customer Applications

Development Kits (SNEUADCDAC16H-DK)

- 2x ES boards allowing for synchronous operation of 2x DAC & 2x ADC, or 4x ADC, or 4x DAC
- High-performance PCB with optimised analogue interfaces
- On-board Raspberry Pi® including easy to use GUI
- Optimised power supply boards for single 12V system operation
- Complete stand-alone system

Each Kit includes

- 2x Evaluation Boards with a soldered ES device on each
- 2x dedicated power supply boards
- Raspberry Pi® with full software package
- 1x Link (backplane) board with system clock sources
- 2x MXP70-2.4mm RF breakout cables for ADC/DAC interfaces
- RF, test and HDMI cables

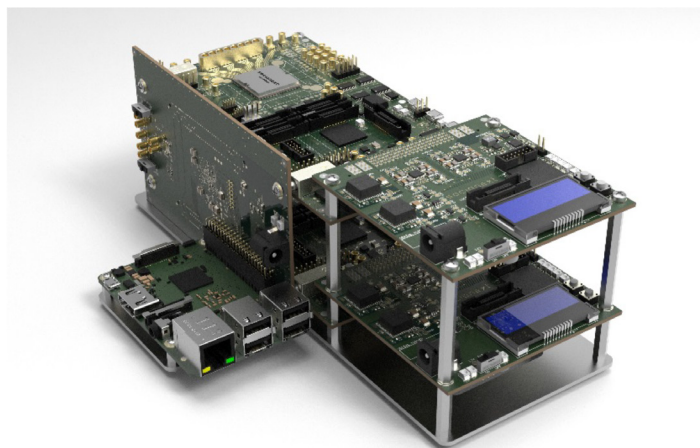
Features

- USB/FPGA control interface (no hardware switches) for simplified set-up
- Synchronization of 2 Evaluation Boards in the kit to emulate 2 x IQ pair
- On-board clock sources
- High-bandwidth 8-way RF connector for ADC/DAC connections
- Power header for attaching auxiliary PSU board
- Optional powering from bench supplies via header
- Test ADCs to measure supplies and temperature

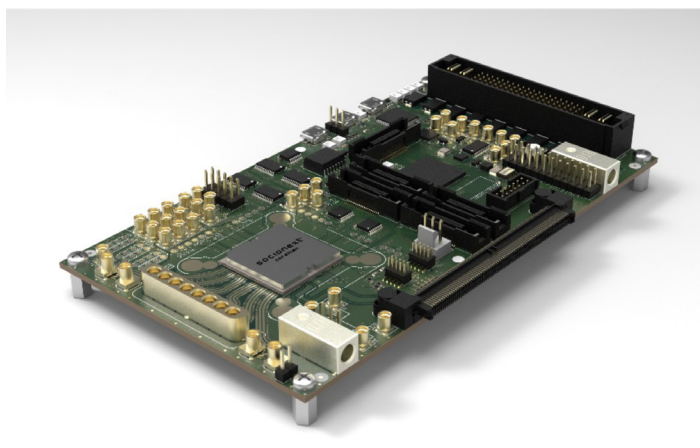
Part Numbers

- SNEUADCDAC16H
- ADC/DAC ES available from IP family information

4-Channel DK



ES Board



This is a preliminary description of the 16nm CHAIS converter IP and is subject to updates and changes.

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