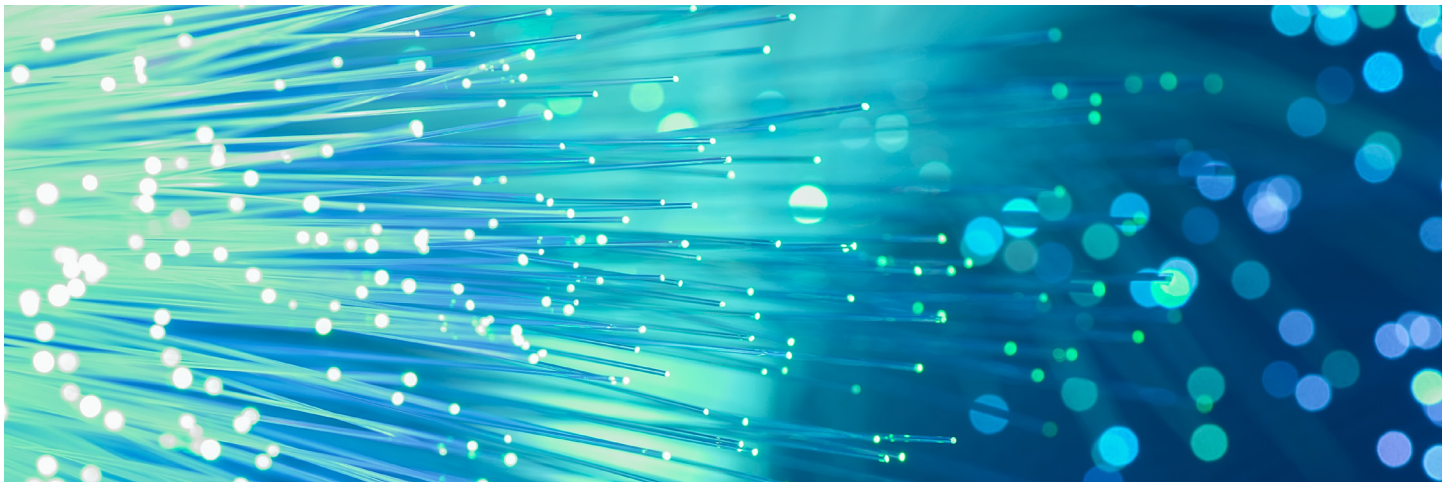
socionext™
for better quality of experience

16nm ADC IP Macro / Test Chip

15 - 103GSa/s 8-bit ADC H-Family



Overview

Socionext has over 40 years' experience and is a leader in state-of-the art system-on-chip technology and provides high-performance SoC designs, serial transceiver technologies and advanced packaging solutions.
Socionext's proprietary CHAIS1 high-speed converter technology, which allows implementation of extremely fast, high-resolution ADC with low power consumption that can be integrated with millions of gates in standard CMOS process, is the latest in a series of IP offerings.

Developed in TSMC 16FF+ process technology, the high-speed ADC has been designed to cover a broad sampling rate range from 15GSa/s to 103GSa/s (ADC H-family). The high-effective resolution and wide-bandwidth characteristics of previous generations of CHAIS are now supported in a smaller process node, enabling lower power SoC solutions for coherent optical transceivers and high-speed test equipment but is also capable of supporting a whole range of other application areas.

1) CHAIS – CHArge-mode Interleaved Sampler technology

ADC IP Macro Basic Features

- Foundry TSMC
- Technology: 16nm FF+
- Sampling rate (Fs): 15-103GSa/s
- Bandwidth (-3d): 0.4*Fs
- Programmable analogue input range: 0.5 – 1.7VPPDIFF
- Fully programmable and high-performance fractional DPLL
- Available in single channel, IQ pair, 2x IQ pair and 4x IQ pair
- Programmable 8, 7 and 6 bit conversion
- Output clock @Fs/128 to digital core per channel
- Fully specified for -5°C to 100°C operation
- APB control interface
- Silicon proven and used in production, immediately available

Deliverables

- Documentation: datasheet, user guides, test report
- Hard macro & integration support
- Abstract LEF and timing LIB files with constraints
- Behavioral verilog model
- Example test bench
- Layout/package guide

Applications

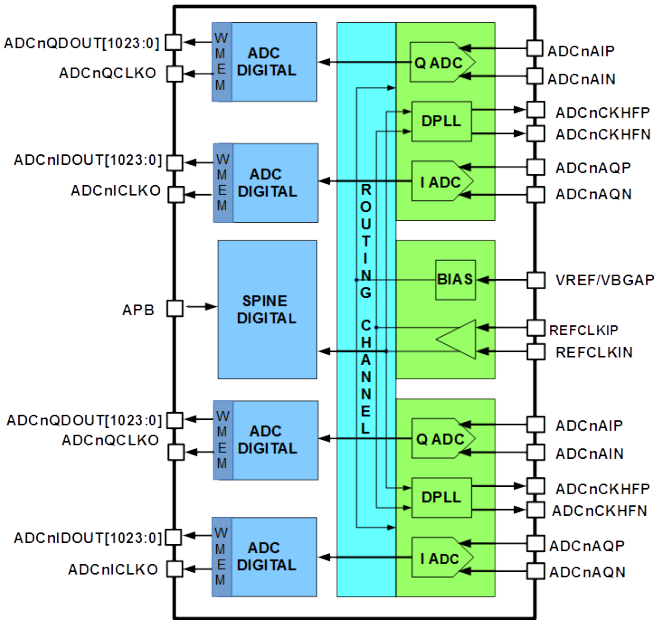
- High-Speed Communication Systems
- Wireline/Optical Networking
- Wireless/Satellite Communication
- Antenna/Phased-Array/MIMO Systems
- Test & Measurement Equipment
- Industrial and Customer Applications

ADC IP Macro (H-Family) Part Numbers

- SNEUADC103H16 - full rate: 60 - 103GSa/s
- SNEUADC051H16 - 1/2 rate of 60 - 103GSa/s resulting in: 30 - 51GSa/s
- SNEUADC025H16 - 1/4 rate of 60 - 103GSa/s resulting in: 15 - 25GSa/s

For more detailed information on the macro family and support, please contact your Socionext representative.

Block Diagram - Example for a 4-channel ADC IP macro



Support

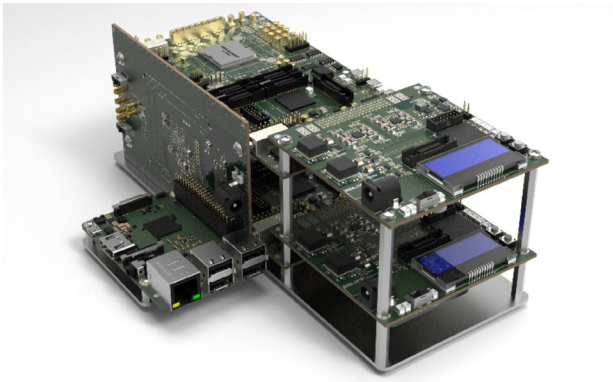
- Development Kit and ADC test chip for customer hands-on experience
- Test program development support
- SI/PI design support

Development Kit

Part Number: SNEUADCDAC16H-DK

- 2x ES boards allowing for synchronous operation of 2x DAC & 2x ADC, or 4x ADC, or 4x DAC
- High-performance PCB with optimised analogue interfaces
- On-board Raspberry Pi® including easy to use GUI
- Complete stand-alone system

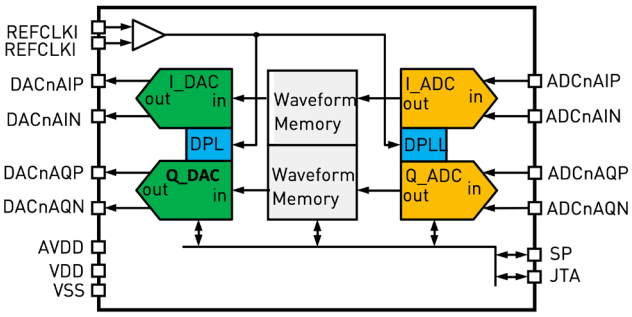
4-Channel DK



Test Chip (ES)

Evaluation of Socionext's 16nm CHAIS converters can be conducted via a customized hardware & software platform. Test chips includes 2 channels (one IQ pair) of the 15-103GSa/s 8-bit ADC H-family and 2 channels (one IQ pair) of the 70-120GSa/s 8-bit DAC H-family.
Each of these channels has a capture RAM (waveform memory) to store 512k x 8-bit samples.
The data transfer from / to the waveform memory is via an industry standard SPI databus running at 3MHz.

4-Channel Test Chip (ES)



This is a preliminary description of the 16nm CHAIS converter IP and is subject to updates and changes.

Socionext Europe GmbH

Pittlerstrasse 47
63225 Langen, Germany
Tel: +49-6103-3745-312
Email: socionext-networking@eu.socionext.com
http://eu.socionext.com

Branch: Socionext Europe GmbH
3 Concorde Park, Concorde Road,
SL6 4FJ, Maidenhead, UK