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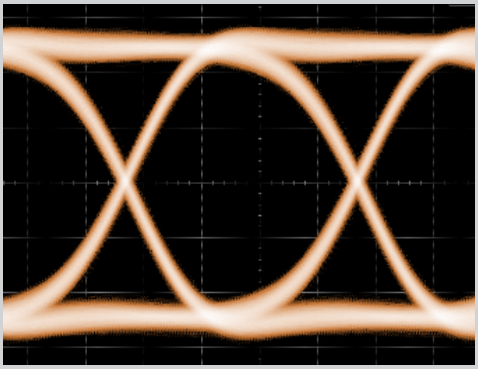
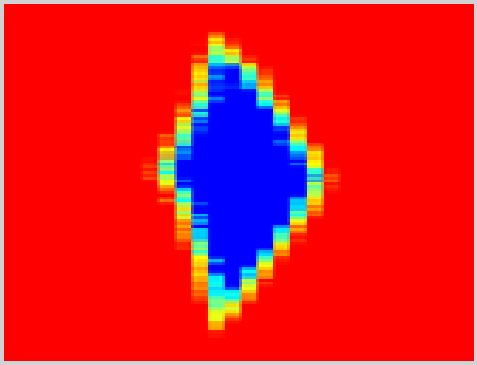
16nm 28G/11Gbps SerDes Macro SNIHS7DTR4VB0



Transmitter Eye Diagram at 28.3 Gbps



Receiver on-chip Eye Diagram at 28.3 Gbps (example)

Key Features

- 4-lane transceiver macro
- Dual-mode operations
  - 28G mode: 25.78 Gbps to 28.30 Gbps
  - 11G mode: 9.95 Gbps to 11.30 Gbps
- Supports chip-to-chip and chip-to-module interfaces defined in CEI-11G, CEI-28G and IEEE 802.3
- Configurable Fractional PLL
- Selectable transmitter equalization
  - 3-tap Feed Forward Equalizer (FFE)
- Adaptive receiver equalization
  - Continuous Time Linear Equalizer (CTLE)
  - 30 TAP equivalent Decision Feedback Equalizer (DFE)
- Asynchronous data transfer using dedicated Clock Data Recovery (CDR) circuit in each receiver
- Macro synchronization capability for low Tx lane to lane skew
- Built-in level shifters for Adaptive Supply Voltage (ASV) technology of customer's logic
- Configurable indicators
  - PLL Lock Detect
  - CDR Loss of Lock Detect
- High testability
  - Built-in PRBS generator and checker
  - Internal serial and parallel loopback
  - On-chip eye monitor
  - IEEE 1149.6 AC boundary SCAN
- Support flip-chip package
- 0.8 V and 0.9 V supplies, TSMC 16FF+ process

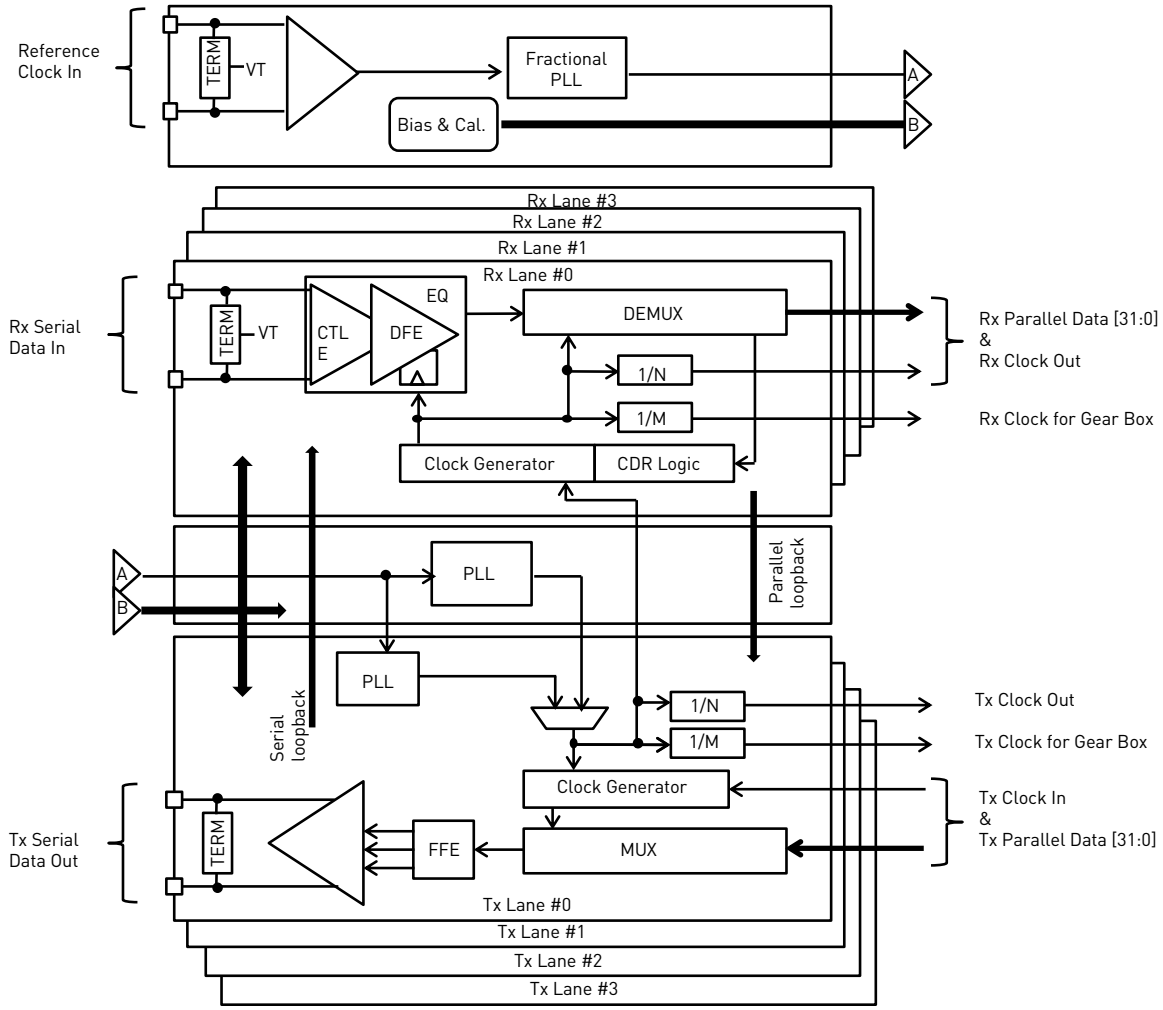
Applications

- High-speed medium reach applications up to 500 mm of typical PCB plus one connector
- Electrical interface in 100 G / 200 G / 400 Gbps broadband optical network
- 10 G, 40 G and 100 Gigabit Ethernet connection with 1 x 10 Gbps, 4 x 10 Gbps, 10 x 10 Gbps and 4 x 25 Gbps
- Next generation 25 G and 400 Gigabit Ethernet connection
- 10 Gbps and 25 Gbps optical module electrical interface
- Proprietary chip-to-chip connections

Benefits

- Easy to increase bandwidth with using multiple SerDes on a chip
- Supports robust data transmission and reduces power on various channels with equalizer
- Contributes customer's low power chip design
- Accepts flexible reference clock frequency range
- Easy to debug customer's boards with built-in PRBS generator / checker, serial loopback, parallel loopback and eye monitor

Product Overview



Block Diagram

Socionext 28G/11Gbps SerDes Macro is a hard macro designed for TSMC 16FF+ CMOS process with 0.8 V and 0.9 V supply voltages.

The SerDes hard macro contains a Fractional PLL which contributes customer's flexible board design for adopting reference clock source, and level-shifters which easily accept customer's digital logic power supply adaptation to optimize performance and power consumption (ASV technology).

The SerDes macro has management registers which configure the SerDes macro for various application. The SerDes macro also has sequencers which allow easy initialization, calibration and reconfiguration.

Low power and wide range PLLs in the SerDes macro are designed to guarantee high quality and robust data transmitting and receiving.

Socionext deliverables of the SerDes macro are industry standard views, complete documentation sets including an evaluation report, accurate channel simulation models (IBIS-AMI model) and a demo board.

Socionext offers high quality SerDes macro solutions for your System on Chip with over 15 years experience in high performance application area.

For more information, visit Socionext web site.

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